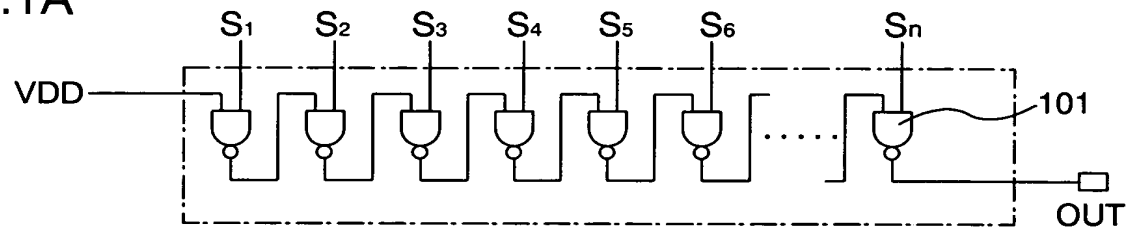
FIG.1A



TESTING CIRCUIT

101 : NAND

FIG.1B

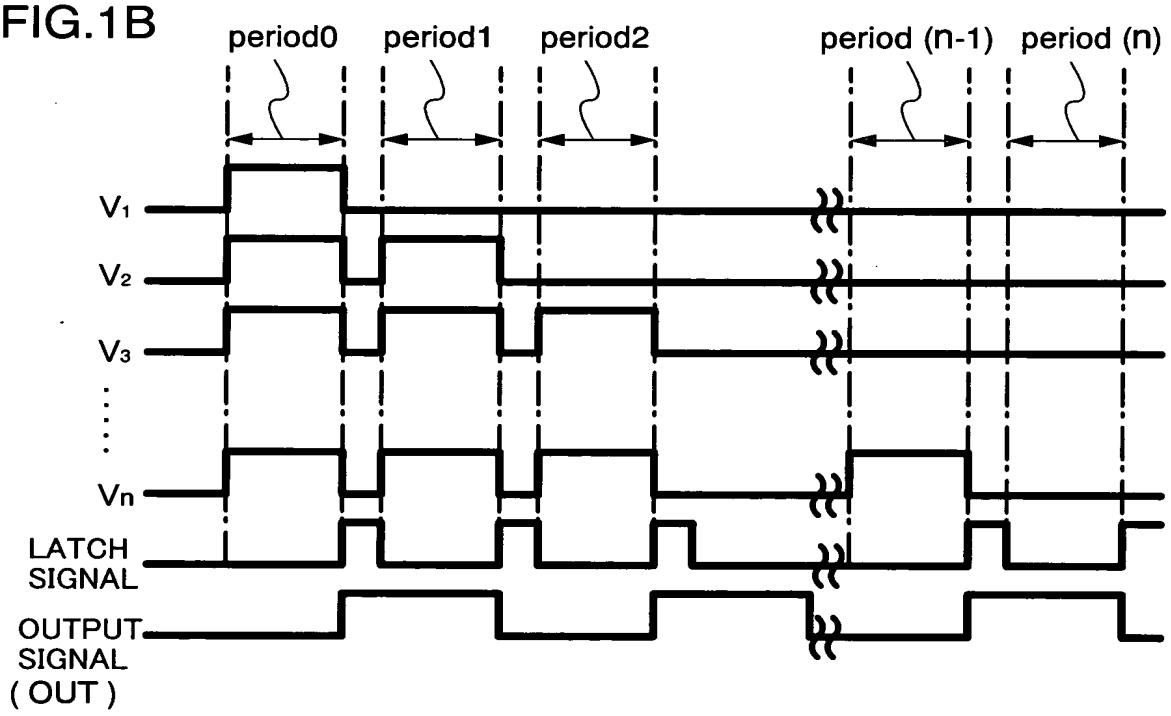


FIG. 2

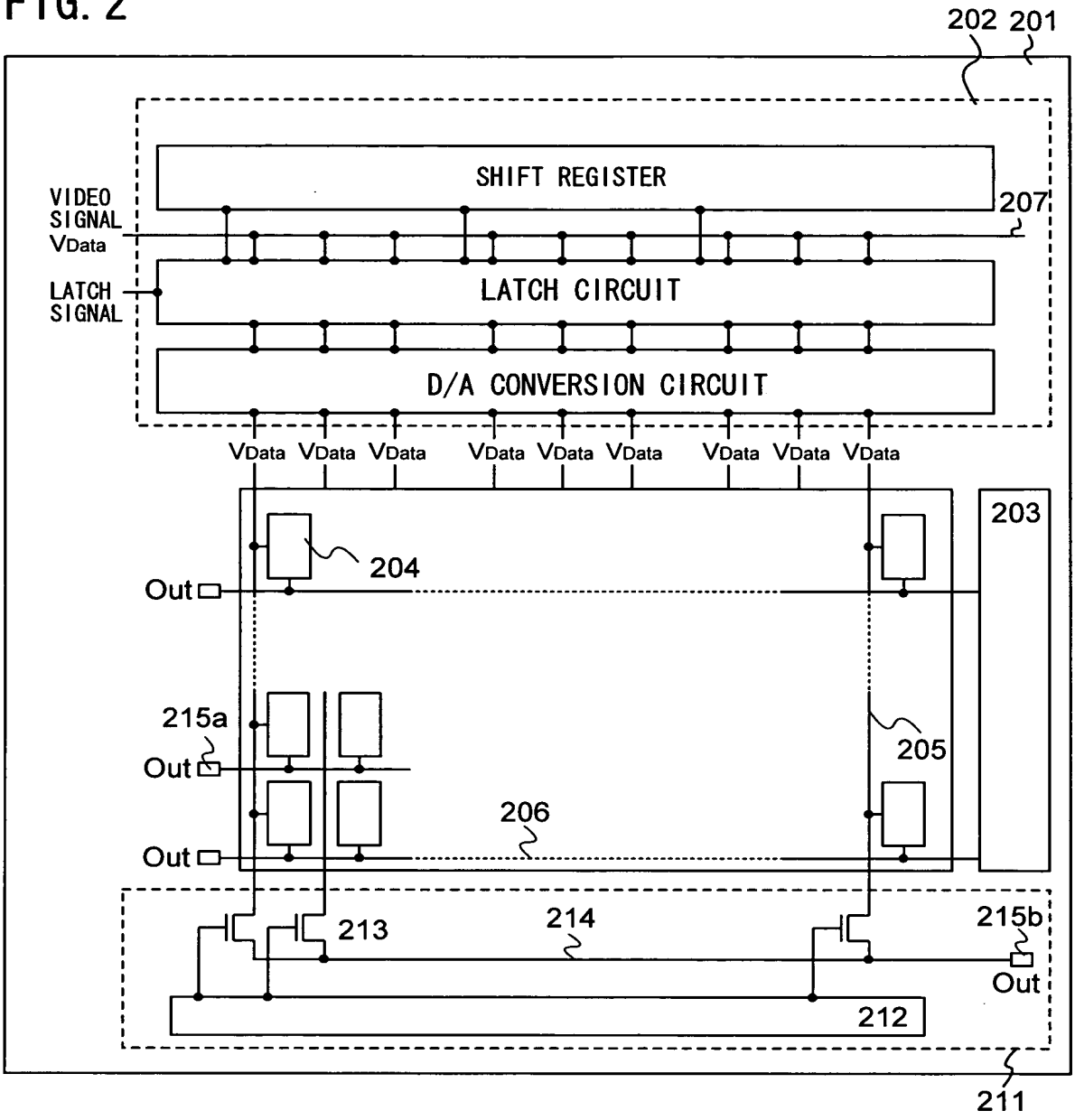

202
201
SHIFT REGISTER
207
VIDEO SIGNAL VData
LATCH SIGNAL
LATCH CIRCUIT
D/A CONVERSION CIRCUIT
VData VData VData VData VData VData VData VData VData
203
204
Out
215a
Out
205
206
Out
213
214
215b
Out
212
211

FIG.3A

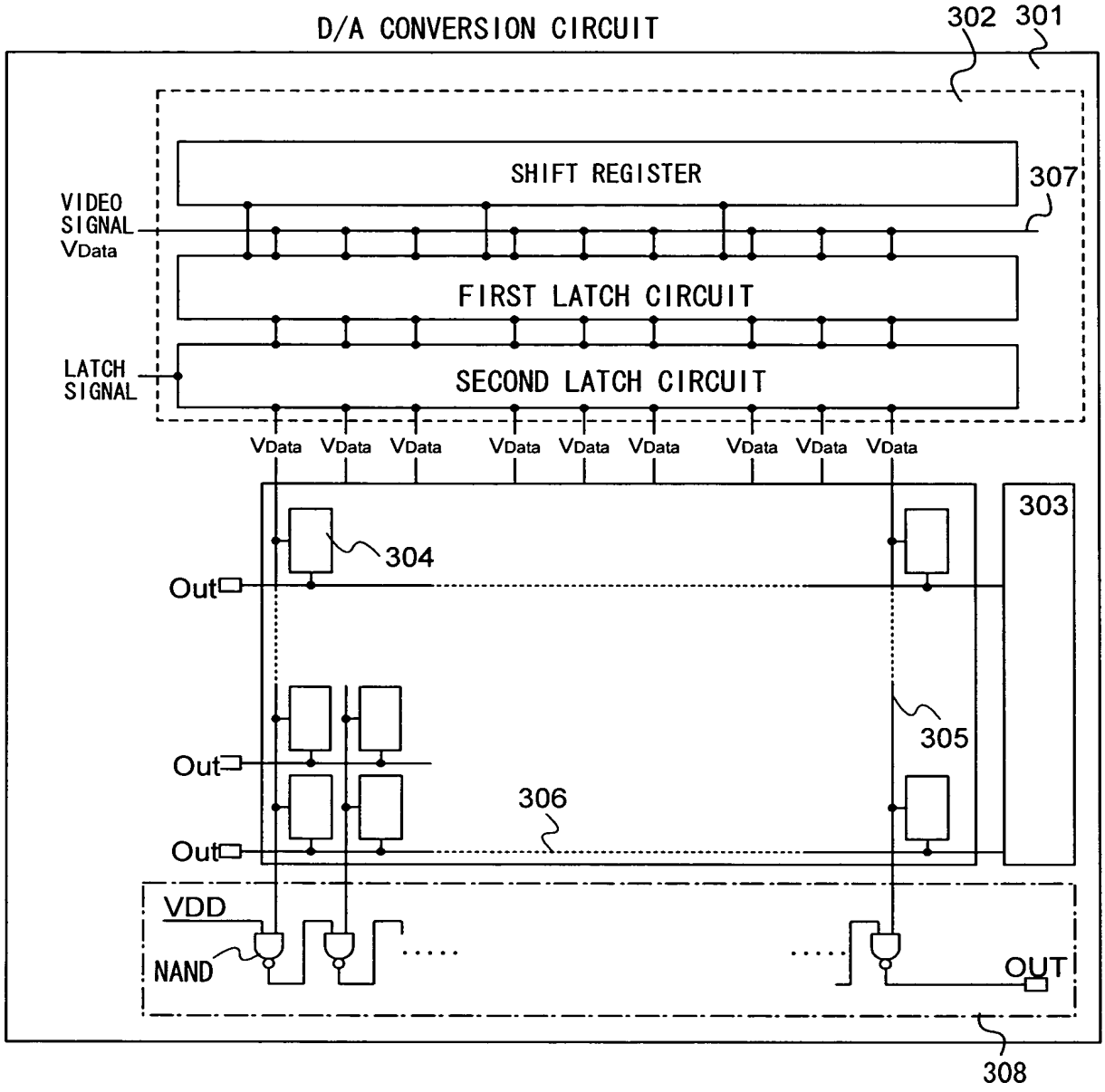

D/A CONVERSION CIRCUIT
302
301
SHIFT REGISTER
307
VIDEO SIGNAL
VData
FIRST LATCH CIRCUIT
LATCH SIGNAL
SECOND LATCH CIRCUIT
VData VData VData VData VData VData VData VData VData
303
304
Out
305
Out
306
Out
VDD
NAND
OUT
308

FIG.3B

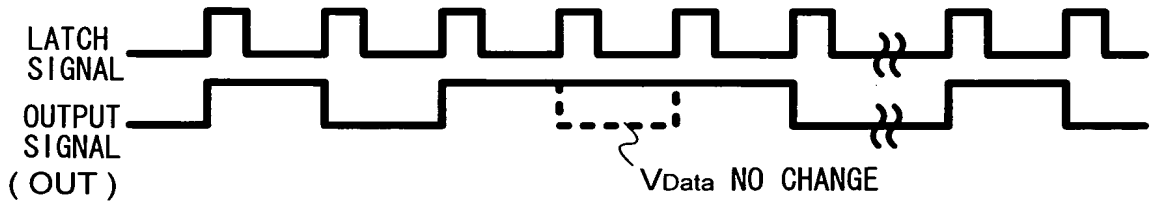

LATCH SIGNAL
OUTPUT SIGNAL
(OUT)
VData NO CHANGE

FIG.4A

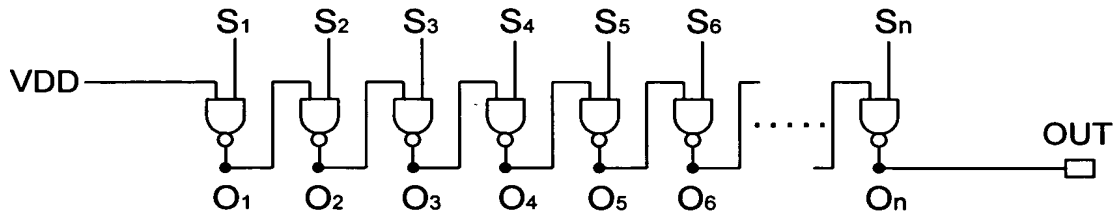


FIG.4B

[n = odd]

	V1	V2	V3	V4	V5	V6	·····	Vn	
NANDOUT	O1	O2	O3	O4	O5	O6	·····	On	
VData	1	1	1	1	1	1	·····	1	401
NANDOUT	0	1	0	1	0	1	·····	0	
VData	1	1	1	0	1	1	·····	1	402
NANDOUT	0	1	0	1	0	1	·····	0	
VData	0	1	1	0	1	1	·····	1	403
NANDOUT	1	0	1	1	0	1	·····	0	
VData	0	0	1	0	1	1	·····	1	404
NANDOUT	1	1	0	1	0	1	·····	0	
VData	0	0	0	1	1	1	·····	1	405
NANDOUT	1	1	1	0	1	0	·····	1	
VData	0	0	0	1	0	1	·····	1	406
NANDOUT	1	1	1	0	1	0	·····	1	
VData	0	0	0	1	0	0	·····	1	407
NANDOUT	1	1	1	0	1	1	·····	0	

FIG.5A

[n = odd]

	V_1	V_2	V_3	V_4	V_5	V_6	·····	V_n	
$NAND_{OUT}$	O_1	O_2	O_3	O_4	O_5	O_6	·····	O_n	
VData	1	1	1	0	1	1	·····	1	501
$NAND_{OUT}$	0	1	0	1	0	1	·····	0	
VData	0	1	1	0	1	1	·····	1	502
$NAND_{OUT}$	1	0	1	1	0	1	·····	0	
VData	0	0	1	0	1	1	·····	1	503
$NAND_{OUT}$	1	1	0	1	0	1	·····	0	
VData	0	0	0	0	1	1	·····	1	504
$NAND_{OUT}$	1	1	1	1	0	1	·····	0	
VData	0	0	0	0	1	1	·····	1	505
$NAND_{OUT}$	1	1	1	1	0	1	·····	0	
VData	0	0	0	0	0	1	·····	1	506
$NAND_{OUT}$	1	1	1	1	1	0	·····	1	

FIG.5B

[n = odd]

	V_1	V_2	V_3	V_4	V_5	V_6	·····	V_n	
$NAND_{OUT}$	O_1	O_2	O_3	O_4	O_5	O_6	·····	O_n	
VData	1	1	1	1	1	1	·····	1	507
$NAND_{OUT}$	0	1	0	1	0	1	·····	0	
VData	0	1	1	1	1	1	·····	1	508
$NAND_{OUT}$	1	0	1	0	1	0	·····	1	
VData	0	0	1	1	1	1	·····	1	509
$NAND_{OUT}$	1	1	0	1	0	1	·····	0	
VData	0	0	0	1	1	1	·····	1	510
$NAND_{OUT}$	1	1	1	0	1	0	·····	1	
VData	0	0	0	1	1	1	·····	1	511
$NAND_{OUT}$	1	1	1	0	1	0	·····	1	
VData	0	0	0	1	0	1	·····	1	512
$NAND_{OUT}$	1	1	1	0	1	0	·····	1	
VData	0	0	0	1	0	0	·····	1	513
$NAND_{OUT}$	1	1	1	0	1	1	·····	0	

FIG. 6A

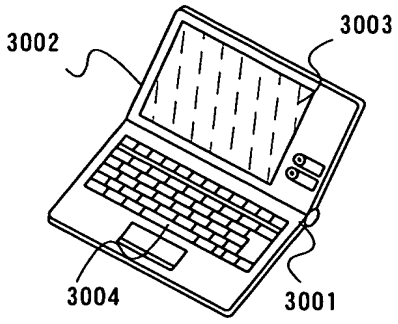


FIG. 6B

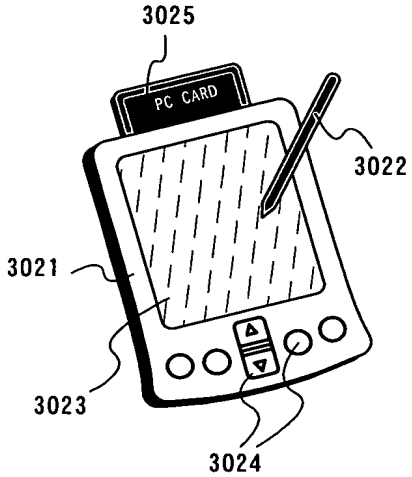


FIG. 6C

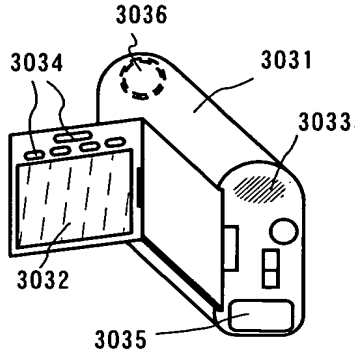


FIG. 6D

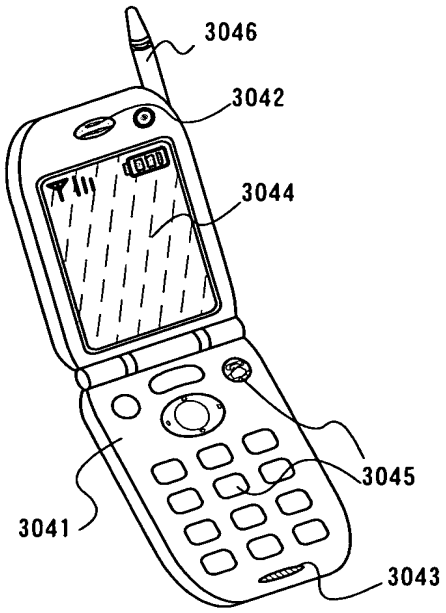


FIG. 6E